REMARKS

Applicants respectfully traverse and request reconsideration.

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,263,448 (Tsern et al.). The Tsern reference is directed to a power control system for a synchronous memory device operating in a standby mode. For example, Tsern describes a problem with previous memory devices wherein additional latency occurs for turning on control logic when exiting the standby power mode of the memory device. As such, as shown for example in FIG. 5, different internal clock domains of a memory are used such as separating out the RAS control logic into a separate clock domain from the CAS control logic. A smaller amount of RAS control logic is left on in a standby power mode to eliminate visible latency from a RAS signal through to data access. Read and write data paths are also in separate clock domains.

In another embodiment, such as that shown in FIG. 9, a memory device dynamically switches between a fast and a slow clock to a memory core, namely one or the other clock speeds, depending upon the needed data bandwidth. The data bandwidth across a memory interface is monitored by, for example, a memory controller. Clock speed is then increased or decreased to one of two clock speeds, namely a fast clock and a slow clock for a memory core.

In contrast to Tsern, Applicants' claimed invention finds use, for example, during non-standby modes, namely during active system modes (see Specification, p. 4, ll. 26-29). The claimed invention selectively activates at least some of a plurality of independent clock signals to a number of memory interface circuits for differing processing engines. Accordingly, multiple independent clock signals are activated at the same time since they are used for a plurality of, for example, memory interface circuits for memory request engines in a graphics controller. The Tsern reference teaches an opposite approach, for a number of reasons. For example, Tsern selects either a single fast or slow clock signal since the clock is a source for core memory. Moreover, Tsern does not teach or suggest selectively activating a plurality of independent clock signals from a divided memory clock as claimed since there are not a plurality of memory interfaces that couple, for example, to a plurality of memory access request engines such as those found, for example, in a graphics processing unit. Accordingly, Applicants respectfully submit

that Tsern fails to teach, among other things, selectively activating at least some of the plurality of independent clock signals in response to received condition data since two or more independent clock signals are not selectively activated from the memory clock for a graphics controller during an active mode as claimed. Accordingly, Applicants respectfully submit that Claim 1 is in condition for allowance.

As to Claim 1, the Office Action cites memory clock divider circuit as being items 60, 68, 86 and 88 of FIG. 5 and item 142 in FIG. 9. Applicants respectfully note that the circuit in Tsern is directed to a memory core and does not appear to selectively activate a plurality of independent clock signals in response to received condition data during an active mode. In addition, Applicants claim a memory clock source for a graphics controller and dividing the memory clock output signals as a plurality of independent clocks to a number of memory interface circuits for differing processing engines, such as those found in a graphics controller. Such a structure is not taught or suggested by the Tsern reference.

Claims 2-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsern et al. As to Claim 2, Official Notice is taken that an engine clock source for video overlay engines, video capture engines and other engines are well known in the art. Applicants respectfully submit that Applicants' invention is not so limited. For example, Claim 2 requires, among other things, a switching circuit coupled to the engine clock source that generates an output signal to a video overlay engine or a video capture engine or other graphics processing engine and a switching circuit that disables the output clock signal based on specific condition data including video overlay enable data, video capture enable data, multimedia port enable data and other data so that the combination of energy savings through engine clock suppression as well as memory clock signals to memory interface circuits for differing processing devices can be achieved. Tsern is silent as to engine clocks and other processing engines, such as video overlay engines. Moreover, Tsern is silent as to a memory clock source for a graphics controller and a memory clock divider circuit that during an active mode, selectively activates some of the plurality of independent clock signals in response to received condition data for memory interface circuits for differing processing engines. Accordingly, Applicants respectfully submit that Claim 2 is in condition for allowance.

Claim 3 requires, among other things, a variable memory clock control circuit that varies the speed of the memory clock based on a type of memory request from a plurality of memory requesters. It appears that the Office Action overlooks some of the claim language. The variable memory clock control circuit of Tsern does not select one of two clock speeds based on a type of memory request, but instead selects one of the two clock speeds for a core memory based on an amount of bandwidth needed as determined by, for example, memory controller. No distinction is made by Tsern as to the type of memory request being used. Accordingly, this claim is also believed to be in condition for allowance.

As to Claim 4, the Office Action cites memory read latch circuits 60, 68, 106 and 80 of FIG. 5 in the Tsern reference. However, Applicants respectfully note that these memory read latch circuits are in the memory core of a memory chip. Moreover, Applicants claim, among other things, a memory read latch control circuit that dynamically activates and de-activates the plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction during an active mode. In addition, items 60 and 68 appear to be control latches, not read latches. In any event, the Tsern reference does not control memory read latches based on detected memory read requests. If this rejection is maintained, Applicants respectfully request a showing as to the column and line number where such is taught in the Tsern reference. In addition, Applicants' memory read latches are not part of a memory core as required by Tsern.

As to Claim 5, Applicants respectfully reassert the relevant remarks made above with respect to Claims 1 and 4, and further note that the claim requires, among other things, that the memory read latch control circuit generates a read latch enable signal and also includes a read data latency compensation circuit and a gating circuit responsive to the memory clock signal operative to selectively enable and disable memory read latches as a function of memory requests. The Office Action cites tclk as an enable signal and 106 as the gating circuit. Applicants respectfully submit that a clock signal is not the enable signal. Moreover, the circuit 106 is an AND gate that is not activated based on a memory read request nor is the data latency compensation circuit operative to compensate for read data latency as claimed.

As to Claim 6, Applicants respectfully reassert the remarks made with respect to Claim 5. The Office Action cites the multiplexer in FIG. 7 as equivalent to that claimed in Claim 6. Applicants respectfully submit that the multiplexer of FIG. 7 merely selects a slower or fast clock that is output to the memory core. In contrast, Applicants claim a multiplexer having an output coupled to a gating circuit and an input coupled to receive the memory clock signal and a second input coupled to receive a memory clock feedback signal. The multiplexer of FIG. 7, among other differences, does not have an input coupled to receive a memory clock feedback signal nor does the multiplexer of Tsern control output of memory clock signal or memory clock feedback signal to emulate clock delay in the circuit layout. Accordingly, this claim is also believed to be in condition for allowance.

As to Claim 7, the Office Action cites logic circuits in FIG. 7. However, the circuits in FIG. 7 are receiver circuits and DLLs and multiplexers. There are no logic circuits coupled to receive different condition data associated with different condition data sources that output corresponding independent clock signals based on received different condition data. Accordingly, this claim is also believed to be in condition for allowance.

As to Claims 8-16, Applicants respectfully reassert the relevant remarks made above with respect to Claims 1-7.

Attached hereto is a marked up version of the changes made to the claims by the current amendment,. The attached page is captioned "Version With Markings to Show Changes Made."

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Once Amended) A power consumption reduction circuit comprising:

a memory clock source for a graphics controller; and

a memory clock divider circuit, operatively coupled to the memory clock source, that generates divided memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode.

8. (Once Amended) A power consumption reduction circuit comprising:

a memory clock source for a graphics controller;[and]

a memory clock divider circuit, operatively coupled to the memory clock source, that generates divided memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition;

[a]an engine clock source operatively coupled to a switching circuit that generates an output engine clock signal that is selectively coupled as a clock signal to each of a plurality of registers associated with at least one of: a video overlay engine, a video capture engine, I2C control logic and a multimedia port, such that the switching circuit disables the output engine clock signal in response to receiving condition data; and

a plurality of memory read latch circuits and a memory read latch control circuit operative to dynamically activate and de-activate the plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction.

13. (Once Amended) A power consumption reduction method comprising:

generating divided memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines;

selectively activating at least some of the plurality of independent clock signals in response to received condition data;

selectively coupling an engine clock signal to each of a plurality of registers associated with at least one of: a video overlay engine, a video capture engine, I2C control logic and a multimedia port to selectively disable the output engine clock signal in response to receiving condition data; and

dynamically activating and de-activating a plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction.